

Vertical Slit Transistor Based Integrated Circuits (VeSTICs): Overview and Highlights of Feasibility Study

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Abstract: In this note, the concept of Vertical Slit Transistor Based Integrated Circuits (VeSTICs) is introduced and its feasibility discussed. VeSTICs paradigm has been conceived in response to the rapidly growing complexity/cost of the traditional bulk-CMOS-based approach and to challenges posed by the nano-scale era. This paradigm is based on strictly regular layouts. The central element of the proposed vision is a new junctionless Vertical Slit Field Effect Transistor (JL VeSFET) with twin independent gates. It is expected that VeSTICs will enable much denser, much easier to design, test and manufacture ICs, as well as, will be 3D-extendable and OPC-free.

I. Introduction

The power/cost/complexity challenges facing next generation high-end logic circuitry sparked development of an alternative to the mainstream approach to digital IC engineering. An approach which could mitigate the consequences of inherent and rapid complexity increase of subsequently introduced new IC technologies. This quest, initially scoped at the small-volume-products using as a starting point the vision presented in [2], has been documented in more than 20 papers, which collectively constitute a blueprint of a new DFM-oriented IC paradigm. This paradigm can address the cost escalation problem, which during recent years has become relevant for almost all silicon providers. This note introduces this paradigm and reports the results of the preliminary experimental runs.

II. VeSTICs Paradigm: the Brief Overview

The paradigm, which we were seeking, was expected to deliver the least expensive transistors and at the same time provide record-breaking performance in some domains. The IC paradigm that was conceived is presented in this paper and referred to as VeSTICs (Vertical Slit-based ICs).

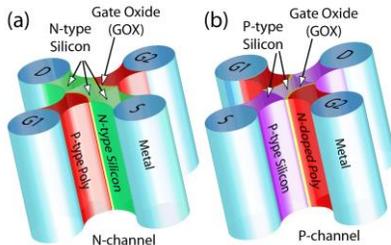


Fig. 1. A complimentary pair of junctionless VeSFETs.

The key component of VeSTICs is VeSFET and its unique geometry, shown in Fig.1. VeSFETs are arranged into an array of geometrically identical transistors shown in Fig. 2 [4]. Such arrays, called VeSTIC Canvases, are envisioned to be

configurable with one-sided or two-sided local interconnect layers and/or by removal or disabling some of devices in the canvas (Fig. 3) [4]

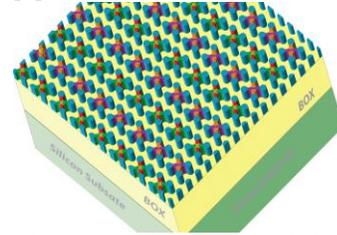


Fig. 2. A segment of the sparse VESTIC canvas, with 64 VeSFETs, located in nodes of orthogonal grid. Grid pitch, in both x and y directions is $4r$, where r is the radius of the smallest possible single, neighbor-less, contact hole which can be delivered by the available infrastructure [4]

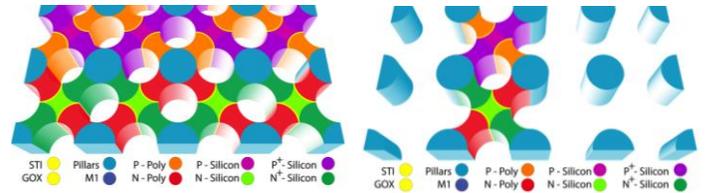


Fig. 3. Left: the densest possible virgin VeSTIC canvas; Right: The canvas customized into an inverter.

VeSTICs follow the Single Circle Device Layout (SCDL) style in which all patterns are drawn with a single spot. SCDL has the potential for vast simplifications of litho process as drastic as elimination of all masks and steppers [4].

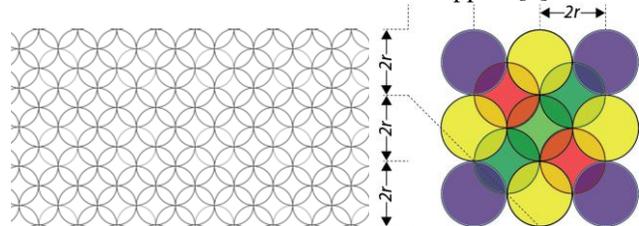


Fig. 4. The Single Circle Device Layout (SCDL) style. On the left: a superposition of all edges on 4 masks needed for fabrication of VeSTIC virgin canvases shown Figs. 2 and 3. On the right: in blue Metal Pillars, in yellow STI, in green n+ and in red p+ poly masks. Each mask is a periodic pattern of identical $2r$ diameter circles that are very convenient to multiexposure litho.

Other important innovations applied in VeSTICs are 4 orientations of metal interconnect: Vertical, Horizontal 45° and 135° [4, 5] and the capability of two-sided routing.

III. Highlights of VeSTIC's Figures of Merit

VeSFET, the nucleus of the entire VeSTICs paradigm has been exhaustively investigated by various simulation schemas

and has been fabricated as special purpose test structures on ordinary SOI substrate. Estimates, computed or eventually measured with the prober on the SOI included: I_{on} , I_{off} , SS, DIBL, frequency of the ring oscillator, dynamic and static powers, as well as, delays of functional blocks. All the obtained data indicate that VeSFET and VeSTICs circuits should deliver superior performances as compared to bulk-CMOS, Fin-FET and FD SOI circuits. In Fig. 5 we present samples of FOMs values, which later will be used to support final conclusions/observations from this discussion.

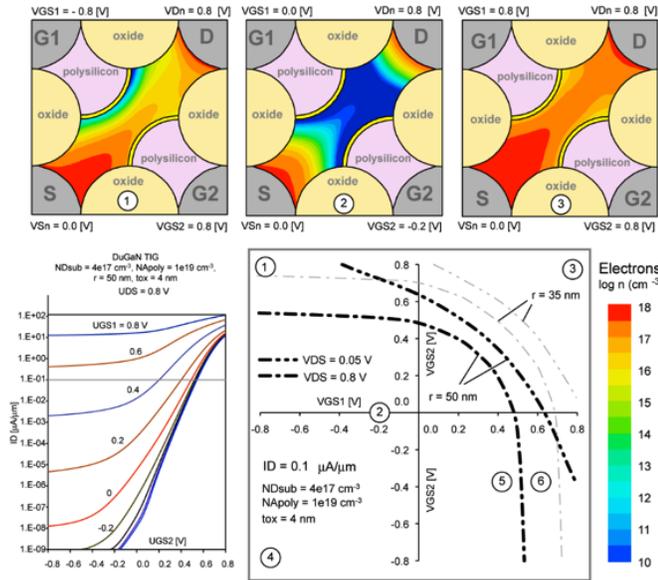


Fig. 5. N-channel VeSFET DC characteristic obtained from TCAD simulations for two independent gates operation. VeSFET is an accumulation type device, with electrically the most effective dynamic control of its threshold voltage. Note the potential for record braking I_{on}/I_{off} ratios.

Results obtained from the real silicon implementation of n-channel VeSFET reported in [6, 7], do confirm VeSFET's superiority in low power applications. For instance, the measured I_{on}/I_{off} ratios greater than 10^9 were obtained by two independent groups located on opposite sides of the globe and earlier hinted by TCAD simulations in Fig. 5.

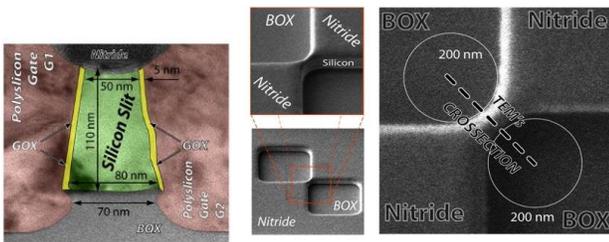


Figure 6: Top and tilted view SEMs of silicon slit region in a fabricated VeSFET test structure (contacts and poly gates are not shown). Fabricated test devices confirmed that very optimistic TCAD I_{off} results (looking at first to good to be true Fig.5) indeed can be delivered by very simple VeSFET architecture. This seems to be especially good news for the entire mobile communication sector of the market. (As we know a big portion of the energy is wasted by leaking transistors "doing nothing".)

Comparisons of benchmark circuits implemented in standard cell style indicate that when operating at maximum speed, the power delay product of VeSFET designs is only 35% of the CMOS designs. When running at the same speed, VeSFET designs consume only 35% dynamic power and 2.6% leakage power of the CMOS-based implementations.

VeSTICs provide an alternative thermal-friendly design choice for 3D integration. VeSTIC chips not only have a much lower power density, but also a better vertical thermal conductivity than their CMOS counterparts. For a VeSFET chip with 10 stacked dice, the temperature increase is only 30% of that for CMOS-based chip. Assuming the same scaling trend for CMOS and VeSFET, VeSFET 3-D chips can postpone the appearance of dark silicon by three technology nodes compared to CMOS implementations [11].

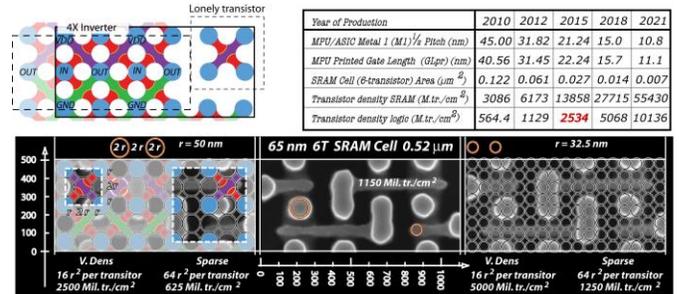


Fig. 7 Superposition of sparse and maximum density canvases on top of 65 nm SRAM indicates that VeSTICs paradigm can achieve the logic circuit density 3 generations ahead of ITRS plan.

IV. Summary

This brief introduction to the IP protected [4,5] VeSTICs vision is not detailed enough to consider all its merits. It is believed, however, that the time is ripe for clear and quick decisions regarding next generation transistor architecture capable of handling anticipated lithography, heat management, and variability challenges. It is in this spirit of an open discussion of all relevant issues that this note is presented for your consideration.

Contributions of Professors M. Marek-Sadowska and A. Pfitzner to this project are acknowledged and appreciated.

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See also: <http://vestics.org>