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Silicon-On-Sapphire, SOS

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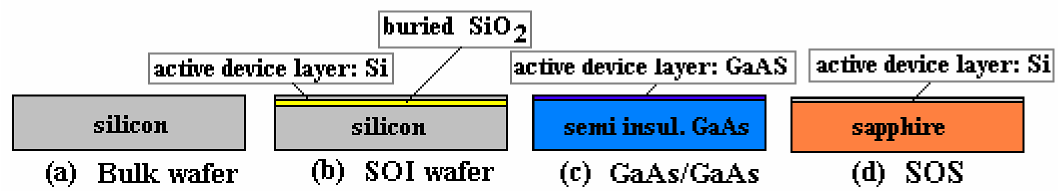
The Silicon-on-Insulator (SOI) substrates used instead of conventional bulk Si wafers are solving several key problems lingering over the cutting edge IC technology (see Semiconductor Note-5 *"Silicon-On-Insulator, SOI"*). For that reason their growing use in advanced Si IC fabrication is inevitable. The first attempt at SOI substrate fabrication, some 30 years ago, was based on the epitaxial deposition of silicon on sapphire resulting in the so-called Silicon-on-Sapphire (SOS) substrates. However, those initial attempts were not successful enough for SOS substrates to meet stringent requirements of large scale IC manufacturing. As a result of a vigorous search for the alternative solutions the current SOI technology based on either wafer bonding or SIMOX processes (see Semiconductor Note-6 *"Fabrication of SOI Wafers"*) was developed.

In the early years, the interest in SOS technology was driven primarily by the needs of military and space applications where robustness and radiation hardness are the key issues. Recently, the interest in SOS technology was revived mainly by the superior performance of CMOS circuitry implemented on SOS substrates in radio frequency (RF) applications such as multi-mode RF switches, mixers, and similar others. This superiority stems from the fact that in the SOS case, an active Si layer is supported by the insulating sapphire wafer (see diagram below), while in the case of other substrates an active device layer is supported by conductive silicon (bulk substrates and SOI), or at best, by the semi-insulating GaAs in the case of GaAs based devices. In high frequency regime, of key importance in wireless communication systems and devices, this difference results in the drastic reduction of signal loses and distortion in ICs built on SOS substrates.



The sapphire (single crystal Al_2O_3), at the resistivity in excess of 10^{16} Ω-cm, is as good of an insulator as SiO_2 is, but features superior to SiO_2 resistance to temperature (melting point of 2300 ^oC as opposed to 1700 ^oC for SiO_2), aggressive chemistries and high energy radiation. Its thermal conductivity is lower than that of Si (0.35 W/cm ^oC vs. 1.3 W/cm ^oC), but is very similar to Ge (0.6 W/cm ^oC) and GaAs (0.45 W/cm ^oC). An added advantage is a high transparency of sapphire (over 80%) to the wavelengths range from about 0.3 µm to about 4 µm. Overall, sapphire is a superior quality substrate for silicon based circuitry not only in terms of the RF performance of the circuit, but also in terms of CMOS integration, scalability, and manufacturability.

Why then with all those advantageous characteristics of sapphire as a substrate for Si CMOS circuitry the SOS technology did no pick up any meaningful momentum in the early years? The reason which brought past development of SOS technology to the halt was a problem with a quality of Si epitaxial layer grown on sapphire. The mismatch between crystal structures of Si (face-centered cubic) and sapphire (hexagonal) makes it virtually impossible to grow defect-free, device quality Si epi layer on sapphire. And while this fundamental limitation remains the same today, ways to work around it were devised in recent years. The trick was accomplished by focusing on the annihilation of structural defects in Si epi layer grown on sapphire rather than on an unachievable goal of growing a defect-free layer. It turns out that through partial amorphization of Si active layer by means of ion implantation followed by thermal treatments resulting in the reconstruction of a single-crystal phase through solid-state epitaxy, defect density in the Si epi layer on sapphire can be reduced to the level warranting successful commercialization of SOS based ICs. Due to these breakthroughs the SOS technology is bound for a significant growth in the years to come. A challenge for the suppliers of sapphire substrates will be to deliver at the reasonable cost the 150 mm and larger wafers with surface finish suitable for epitaxial deposition of silicon.