Fabrication of SOI Wafers

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As Note No. 5 implies Silicon-On-Insulator (SOI) wafers are bound to play a key role in next generations CMOS nanochips technology. This Note describes techniques used to form such SOI wafers in which thin layer of oxide (typically less than 100 nm thick) is "buried" in the Si substrate.

Two main, conceptually very different, thrusts in SOI fabrication have emerged after more than two decades of attempts to fabricate functional single-crystal Si substrates on an insulator. First is based on the concept of implanting oxygen atoms into bulk Si wafer and is known as SIMOX (Separation by IMplantation of OXygen) process. Second, exploits technology of wafer bonding followed by the removal of excess silicon from one of the wafers. Both approaches allow manufacture of wafers up to 200 mm in diameter.

As shown in Fig. 1 in the SIMOX process starting wafer is a conventional "bulk" wafer. Implantation of oxygen into such wafer is then carried out. Implant energy is used to control projected range (depth of penetration) of oxygen ions in Si, and hence, thickness of the oxygen-free layer of silicon above the

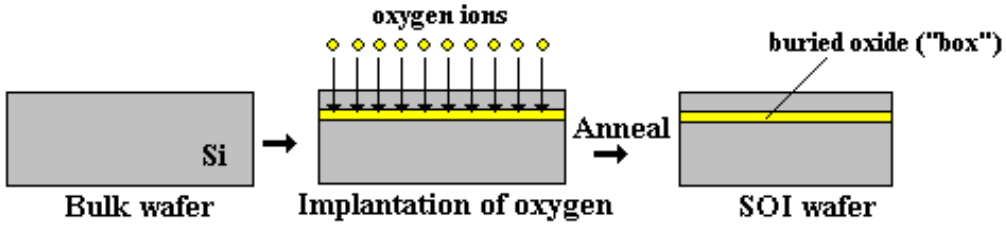

Fig. 1

implanted region (active Si layer). Following implantation wafer is subjected to thermal treatment needed to anneal out implantation damage in the active Si layer as well as to enforce permanent Si-O bonding in the implanted region.

Second approach is based on the well established technology of wafer bonding. As seen in Fig. 2 two oxidized Si wafers are pressed against each other at elevated temperature and as a result are permanently

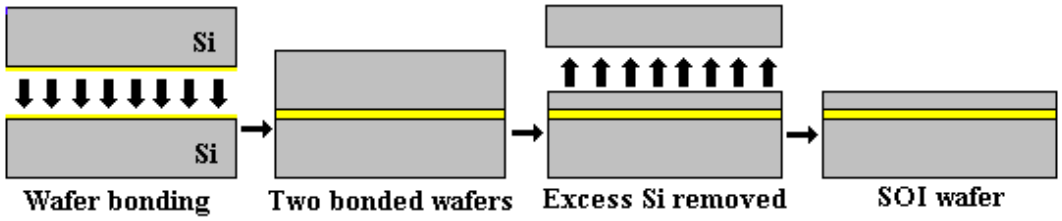

Fig. 2

bonded. Oxide in the bonding plane is to become a buried oxide in the future SOI substrate. Now the excess silicon in one of the wafers ("device wafer") must be removed so that desired thickness of the active Si layer is obtained. This can be accomplished in the variety of ways. The least desirable is etching away or grinding of excess silicon because too much of high quality material is wasted. More advanced methods involve preparation of the "device wafer" prior to bonding in such way that after bonding upper part of the wafer can be separated from the substrate without any damage (hence, can be reused). Well established is the process called "smart cut". In this case "device wafer" prior to bonding is implanted with hydrogen at the depth corresponding to the desired thickness of an active Si layer in the future SOI wafer. Subsequent bonding is followed by the heat treatment at about 500 ^{o}C as a result of which "device wafer" breaks along highly stressed hydrogen implanted region parallel to the interface. The split-off wafer is removed and SOI substrate is formed. Conceptually the same but using different method to induce splitting of the "device wafer" is the process known as ELTRAN (Epitaxial Layer TRANsfer).