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Silicon-on-Insulator (SOI)

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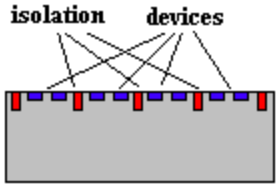
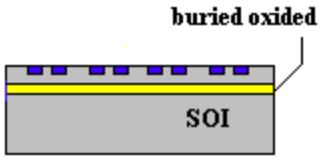
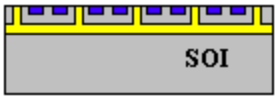
With physical separation between individual devices in ultra-high density CMOS integrated circuits measured in nanometers, proper electrical isolation between them is a key challenge. The SOI (Silicon-On-Insulator) substrate wafers, as opposed to conventional bulk wafers, not only solve the problem of electrical isolation between adjacent devices but also allow innovative device layouts resulting in significantly better than in the case of bulk substrates performance of CMOS circuitry. Hence, SOI substrates rapidly become an important element of the advanced silicon IC technology.



Bulk Si wafer
Fig. 1



SOI Si wafer
Fig. 2

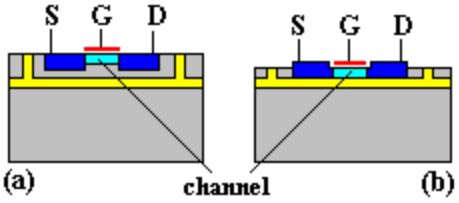


SOI Si wafer
Fig. 3

Figure 1 shows cross-section of a bulk wafer in which individual devices (e.g. PMOSFETs and NMOSFETs in CMOS cell) are isolated by LOCOS isolation or trench isolation (regions in red). By creating a substrate in which very thin layer of oxide is buried underneath the surface, Fig. 2, (see Note No.6 for SOI substrate fabrication techniques) superior isolation between devices is possible. It is accomplished by etching off Si between devices and refilling created narrow trenches with oxide. As a result each among millions of devices comprising a circuit is literally embedded in the oxide (Fig. 3). This not only eliminates leakage current between devices but also reduces parasitic capacitances associated with source and drain regions and results in the faster switching device. One more gain is an increased over bulk wafers radiation hardness of CMOS circuitry built into SOI wafers.

Further improvement in the performance of CMOS circuit on SOI substrate can be accomplished by reducing thickness of the Si active layer, i.e. layer of Si on top of buried oxide. In Fig. 4 the same MOSFET structure is formed in the thicker (Fig. 4a) and thinner (Fig. 4b) active layer. In the latter case

Fig. 4



the layer is so thin that both source (S) and drain (D) regions, as well as channel, expand across the active layer to the buried oxide. Significant performance gains result from implementation of such "Fully Depleted" SOI (FDSOI). Most notably leakage currents of source and drain junctions are drastically reduced. Hence, less power is dissipated into the substrate and premature destruction of device from overheating is prevented. Also, parasitic capacitances associated with source, drain and channel regions are essentially eliminated with increase in the device switching speed resulting.

Yet additional gain in performance of fully depleted SOI CMOS can be achieved by using strained silicon (see Note No.7) as an active layer on top of buried oxide. In this case channel is induced in the strained Si in which electrons feature higher mobility as compared to mobility in standard (relaxed) Si. This obviously leads to the faster switching CMOS cell.