Transistor (R)Evolution

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The concept of a surface field effect transistor, predecessor of the modern MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor), was proposed by J. E Lilinfeld in 1930. It was not until late 60's, however, at which time silicon technology has become mature enough to realize MOS gate stacks based on thermal SiO_2-Si framework that the large scale commercialization of MOSFET technology took place. Since then MOSFET has become a device of choice for an array of digital integrated circuits with microprocessors and DRAMs leading the field. A growth in microelectronics technology that followed was driven primarily by the need to build MOSFETs that would work faster and more efficiently. To meet this challenge MOSFET was continuously evolving toward reduced gate length which in turn was enforcing other changes in the MOSFET design needed to maintain it operational at the scaled down geometry. In the meantime significant improvement in the performance of MOS ICs was accomplished by replacing N-MOSFET based circuitry with CMOS (Complementary MOS) technology.

The arsenal of evolutionary modifications in the MOSFET design and processes needed to maintain expected growth is about to be depleted. Hence, the industry has no other choice but to subject a basic MOSFET (Fig. 1) to an overhaul that will include not only modifications of the device geometry, but will also bring new materials and different Si substrates to the picture.

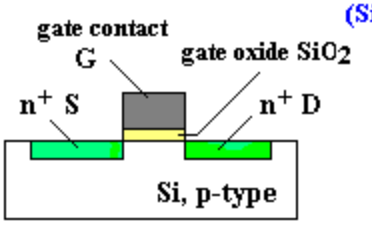

Fig. 1

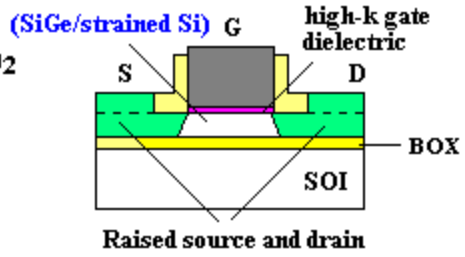

Fig. 2

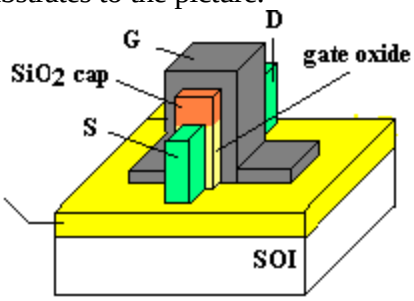

Fig. 3

Figure 2 shows cross-section of the MOS transistor that illustrates changes that can be made to improve its performance. To reduce leakage current device is formed on fully depleted SOI substrates (see SN-5) as opposed to bulk Si wafer in Fig.1. It features raised source and drain, but the most drastic modification is a replacement of SiO_2 gate oxide with a dielectric featuring higher than SiO_2 dielectric constant (see SN-1). This change will enforce switch from poly-Si to a metal as a gate contact. Further improvements in device performance will be possible by increasing electron mobility in the channel through the use of strained silicon formed on SiGe in SGOI substrate instead of Si in a conventional SOI substrate.

Once modifications of a single-gate planar MOSFET (Figs.1 and 2) will be fully exploited a switch to a double-gate configuration exemplified in Fig. 3 by the FinFET structure will have to take place. In this configuration an ultra-narrow silicon "fin" with S and D at its two ends is formed on SOI substrate to act as a fully depleted channel. It has gate oxide and contacts on both sides for a superior control of the drive current. This, and similar innovative designs will push performance of the MOSFET to the new limits. However, commercial materialization of these concepts requires technological breakthroughs that will rewrite the book on MOS technology.