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High-k dielectric? Low-k dielectric?

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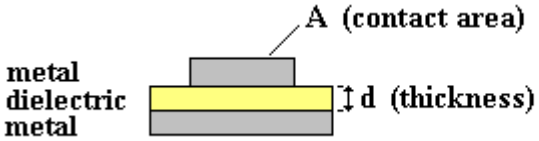
The dielectric constant, k, is a parameter defining ability of material to store charge. Consequently, it also defines capacitance, C, of any capacitor comprising of a layer of dielectric sandwiched between two metal plates. In the figure below size of the upper plate defines area of the capacitor contact (A).



$$C = \frac{\varepsilon_0 k A}{d}$$

All other parameters equal, k would determine capacitance of the above structure, or in other words, it would define the extent of capacitive coupling between two conducting plates – with "high"-k dielectric such coupling would be strong, and with "low"-k dielectric being obviously weak. In Si technology the reference is a value of k of silicon dioxide, SiO_2, which is 3.9. Dielectrics featuring k>3.9 are referred to as "high"-k dielectric while dielectric featuring k<3.9 are defined as "low"-k dielectrics.

In cutting edge silicon nanoelectronics both high- and low-k dielectrics are needed to implement fully functional very high-density integrated circuit, although, for drastically different reasons. High-k dielectrics are needed in MOS gate stacks to maintain sufficiently high capacitance of the metal (gate)-dielectric-Si structure in MOS/CMOS transistors (Fig. 2). Due to the continued scaling of the channel length (L), and hence reduced gate area A, the need to maintain sufficient capacitance of the MOS gate stack was met by gradual decrease of the thickness of SiO_2 gate oxide (see Eq.1). Obviously such scaling

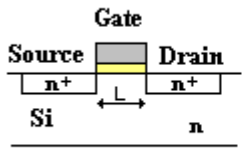


Fig. 2

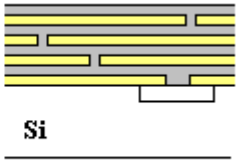


Fig. 3

cannot continue indefinitely as at certain point gate oxide will become so thin (thinner than about 1 nm) that, due to excessive tunneling current, it would stop playing role of an insulator. Hence, dielectric featuring k higher than 3.9, i.e. one assuring same capacitive coupling but at the larger physical thickness of the film, must be used instead of SiO_2 as a gate dielectric in advanced MOS/CMOS integrated circuits.

On the opposite end of the spectrum finds itself a multi-layer metallization scheme in which inter-layer-dielectric (ILD) is used to electrically insulate metal lines. In this case it is of critical importance that the capacitive coupling between adjacent interconnect lines (Fig. 3) is as limited as possible. Hence, a low-k dielectric must be used to assure as little capacitive coupling (low "cross-talk") between interconnect lines as possible.

Whether the problem is with high-k dielectrics for MOS gates or low-k dielectrics for ILDs, lack of viable technical solutions in either of these areas will bring any future progress in mainstream silicon technology to a halt.